Torus Based New Fault-Tolerant Interconnection Network For Parallel Systems

Laxminath Tripathy
Department of CSE, ITER, Siksha 'O' Anusandhan University, Bhubaneswar, India

Abstract:
In this paper, a Torus based new fault-tolerant interconnection network called Fully Twisted Torus (FTT) has been proposed. The proposed interconnection network is a simple and regular structure. It is highly scalable. This network has good fault-tolerance capability. The topological properties like node degree, network diameter, bisection width, network cost, and packing density of the proposed network are investigated and compared with other contemporary networks. The FTT is better than Mesh, Torus, MCR, and OUC in terms of node degree, network diameter, average distance, packing density, bisection width, and network cost. The routing techniques in two distinct cases (i) Fault-free routing (ii) Fault-tolerant routing are proposed. The FTT offers a high degree of fault tolerance.
Keywords: Diameter, Cost, Packing Density, Static routing, Bisection Width, Fault-tolerant routing
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1. Introduction

The interconnection networks are the critical elements in parallel systems. Many topologies for interconnection networks have been developed in the past. The important ones among them include Mesh and Torus. Over the years, the Mesh and Torus topologies have gained significant popularity in parallel computing applications in various machines used for commercial and academic purposes. This is because of balancing the trade-off between the diameter of the network and hardware cost.The Torus topology is also referred to as the k-ary-n-cubes, where k represents the number of nodes in each dimension and *n* represents the number of dimensions in a network topology. The torus is a symmetric topology because it looks the same from every node. This topology also provides better load balancing. It takes advantage of communication locality in parallel systems [5]. In [6], the Torus has been claimed to be a cost-effective and fault-tolerant network. Due to its uniform degree, small diameter, and faulttolerance, the torus can be the better option for interconnection purposes in parallel systems. A system can be highly scalable if it has a constant node degree [25].

Due to high path diversity, many nonoverlapping paths between any node pairs can be used duringthe routing ofpackets to manage the traffic [34]. The traffic can be balanced by distributing packets over the non-overlapping redundant paths. This torus is highly reliable, scalable,and supports bidirectional signaling. Itis also a popular topology in the top 500 lists such as the 3D torus topology in Oak Ridge National Laboratory’ s Titan [7], the 5D torus topology in Lawrence Livermore National Laboratory’ s Sequoia [8,29], and the 6D torus topology in Riken’ s K computer [9]. It is used in Intel TFLOPS supercomputer [1], DASH multiprocessor [2], Alpha 21364 [3], and BlueGene/L supercomputer [4].

Many researchers have given the focus on the improvement of the topological structure of the torus and efficient routing techniques. Therefore, the Torus network needs to be improved to maintain uniform node degree, small diameter, and less hardware complexity. The design of multidimensional torus like 5D torus networks makes it difficult to analyze the proper network utilization due to ill-formed communication patterns since the spatial understanding of humans is limited to 3-Ds[29].

In this paper, a new fault-tolerant interconnection network called Fully Twisted Torus (FTT) has been proposed. The rest of the current paper is organized as follows: In Section 2, a detail description of existing work ispresented. The proposed network along with its topological properties and routing are discussed in Sections 3 and 4 respectively. In Section 5, the performance of the proposed network has been compared with the existing networks. The concluding remarks are presented in Section 6.

2. Related Works

In the past, many interconnection networks have been designed for parallel systems. Those include Mesh [10], Torus [6], Chordal Ring [11], Hierarchical Ring[12], THIN[13], DL(2m)[14] Rgrid[15], XMesh[16], Torus embedded Hypercube [17], Meshes of Torus [18], Mesh connected Ring(MCR) [13], and OUC[19]. The Mesh and Torus networks are frequently used as interconnection networks for parallel systems. These are also suitable for designing network on chip (NoC). The network degree of the Torus is 4 and the mesh-connected ring (MCR) is 3. Though the MCR is better than Mesh and Torus networks in terms of topological parameters, the degree of both MCR and Mesh are not uniform i.e., nodes present in boundary positions have a different degree than the nodes present in interior positions. Further, considerable research effects have been directed at developing many variations of the Torus network. Those are SD Torus [20], TM topology [21], Dia-Torus [22], xxtorus [23], and CCTorus[24], three-tier Delaunay Network[32]. The variations of all the said Torus networks have different node degrees and small diameter than the parent Torus network. The topological structure parent topology has beenmodified and shown these variations are better.

Authors in [28] proposed a routing algorithm called binary optical routing algorithm(BORA) which proved that this is abetter choice than conventional XY routing in a torus network in terms of network throughput and latency. Authors in [30] proposed a rectangular twisted torus in which the torus is in a rectangular structure and it is not uniform in size though the diameter is reduced.

The Cross-By-Pass-Torus is obtained from the modification of the torus which increases the performance of the Cross-By-PassMesh topology. This design has better features of the Cross-By-Pass-Mesh and Torus, to reduce the diameter of torus topology [35]. However, the number of links is more than the torus network and the node degree is different in different positionsi.e. varies from 5 to 9 depending upon the position of the node.

The XTorus and CC torus topology are derived from the torus by adding more links to the center nodes with the rest of the nodes which gives rise to the cost of networks and non-uniformity in the degree of the network.

The hardware cost of a network per node is directly related to the degree of a node. So further improvements can be done to achieve better performance by keeping constant node degree. Therefore, the Torus network needs to be improved to have uniform node degree, small diameter, and less hardware complexity.

3. Proposed Network: Fully Twisted Torus Network (Ftt)

In this section, we propose a new fault-tolerant network called Fully Twisted Torus (FTT). The proposed interconnection topology is similar to torus topology except for the connection patterns of wraparound links which are connected in twisted form. The position of a node is represented by two coordinates. The first coordinate represents the position of nodes along x and the second coordinate represents along y direction. The connection patterns of a node A (x_1, y_1) in FTT for sizen×n is as follows:

1. If x_1 and y_1! = n-1, the position of four connected nodesis

$B(x_1+1, y_1)$, $C(x_1, y_1+1)$, $D(x_1-1, y_1)$, $E(x_1,y_1-1)$.

2. If position of A is $(0, y_1)$
   $B(n-1, t_1)$, $C(1,y_1)$, $D(0,y_1+1)$, $E(0,y_1-1)$
3. If the position of A is $(x_1, 0)$, A is connected directly to the following nodes
   $B(t_2,n-1)$,$C(x_1+1,0)$,$D(x_1-1,0)$, $E(x_1,y_1+1)$
4. If node A is at (0,0) position then the connected nodes are in following positions
   B(t,n-1),C(n-1,t),D(1,0),E(0,1).

The value of t_1 in case of 2 is Mid+y_1 mod n. Similarly, the value of t_2 in case 3 is Mid+ x_1 and in case 4 value of t = Mid where mod is mathematical module operation and the Mid =$\lfloor n/2 \rfloor$. For FTT of size n=8, the wraparound connection along xdirection is as follows: wraparound with (0+3) mod 6=3, i.e 0 is connected to 3 = 0---3. Similarly, the other connections are 1---4, 2---4, 3---5, 4---0, 5---2 The proposed network FTT with n=6 is shown in Fig.1.

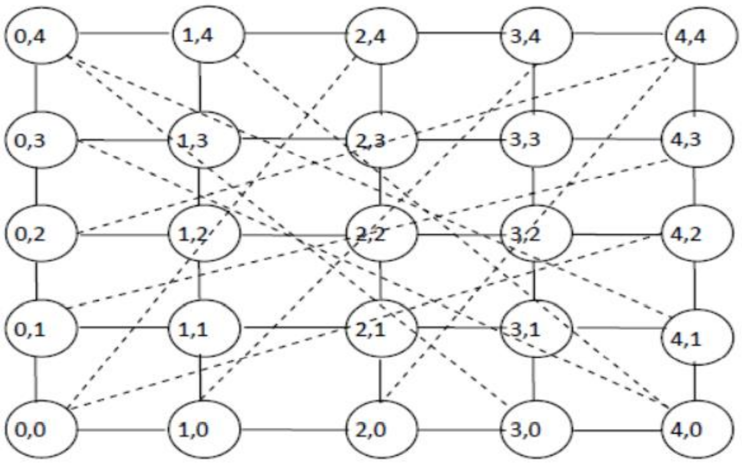

Figure 1: Fully Twisted Torus (FTT) for n=6

4. The Topological Properties Of The Proposed Network (Ftt)

In this subsection, the different topological properties of FTT have been presented. The important topological properties of FTT of n×n size are as follows.

The FTT has a uniform node degree. Its structure is the same as the torus but the only wraparound connections are present in the rotated form. It has same degree as of Torus network.

Theorem 1

The diameter of FTT is n-2.

Proof: The diameter is the farthest distance between any two nodes. The nodes present between two endpoints along any axis have the longest distance than any other pair of nodes. The diameter of the proposed network is n-2. For example, the two nodes at (0,0) and (0,5) of Fig.1 has distance 4 which is computed from the path along with wraparound connections. Hence the proof.

Theorem 2

The bisection width of FTT is 3n.

Proof: From the definition of the topology, it is clear that the wraparound connections start from mid position onwards. So, all wraparound connections are crossing the mid position along both X and Y axis. As bisection width divides the network into two halves so, the total number of links crossing mid position is the total number of wraparound connections and the total number of links in the same direction. The total numbers of wraparound connections are 2n and the total number of links in any direction is n. Hence, the bisection width is 2n+n=3n. Hence the proof.

Theorem 3

The cost of FTT is 4(n-2).

Proof: The cost of the network can be obtained from the product of degree and diameter. As the degree of FTT is 4 and the network diameter is n-2 so, the cost is 4(n-2). Hence the proof.

Theorem 4

The packing density of FTT is $\frac{n^2}{4(n-2)}$.

Proof: It can be obtained from the size of the network per unit cost. The size of n × n FTT is n2. From Theorem 3, the cost is 4(n-2). So, the packing density is $\frac{n^2}{4(n-2)}$. Hence the proof.

5. ROUTING IN FULLY TWISTED TORUS

Here, the routing in two different situations is considered for the proposed network FTT. The routing in FTT is simple and the computation is straightforward. For the selection of a path, the following conventions are used.

wx= wraparound connection along x axis.

wy= wraparound connection along y axis.

Routing in FTT in Fault-free situation (Static Routing)

Based on the difference between the node positions of the source and destination, the path will be selected for routing. Assume the position of the source and destinations are (x_1, y_1) and (x_k, y_k) respectively. Let the diameter of the network is D. The path along x-axis, y-axis, w_x, and w_y is selected as per the following procedure.

A. Route_source (x_1,y_1) and Destination (x_k,y_k)

Algorithm:

1. Compute Δx, Δy, and s where $\Delta x=x_1-x_k$, $\Delta y=y_1-y_k$ and $s=|\Delta x|+|\Delta y|$.
2. If ($s \geq D$)

```
    if (|Δx|>|Δy|)
        If(y1=0)
            If(x1>Mid))
                Set path= (xn-1 –Mid)wy
            else
             Set path=  –x1wy   //-ve sign for left direction
         else if(y1>mid)
              Set path=(yn-1-y1)wy
else
                set path= -y1wy // -ve sign for downward direction
else if(if(x1=0)
         if(y1>Mid))
                Set path= (yn-1–Mid)wx
          else
              Set path=  –y1wx  //-ve sign for downward direction
       else if(x1>Mid)
           Set path=(xn-1-x1)wx
            else set path= -x1wx // -ve sign for left direction
```

3. Update x_1,y_1 to the current position and go to step 1
4. If ($s \leq D$)

```
    if(x1≤ xk)
      {
      Path= Δx //  Δx hops towards right
      if(y1≤ yk}
```

```
        Path=Δy // Δy hops in the upward direction
        else
          Path= -Δy //Δy hops in the downward direction
    }
   else
    {
       path= -Δx // Δx hops towards left.
       if(y1≤ yk)
           path=Δy // Δy hops in an upward direction
       else path= -Δy // Δy hops in downward direction
    }
```

B. Routing in FTT in Faulty situation (Fault-Tolerant Routing)

As there are many pathsrhat exist between any source and destination node so, the fault can be tolerated by rerouting of the message in any of the alternate path. The fault may be at any link along x direction, y direction, w_x or w_y (wraparound connection along x axis or y axis). Depending upon the position of the destination and type of link or node fault, the tolerance will be done according to the following procedure. Let the current position of the node is node(i,j) and next location during routing is node(k,l).

Algorithm:

Case 1: For any of link along x direction is faulty

```
if (i<k)
 if (j<(n-1)
     Next positions are (i,j+1),(i+1,j+1),and (i+1,j-1)
 else
    Next positions are (i,j-1),(i+1,j-1),and (i+1,j+1)
 else if(j<n-1)
   Next positions are (i, j+1),(i-1, j+1),and (i-1,j-1)
   else
    Next positions are (i,j-1),(i-1,j-1),and (i-1,j+1)
```

Case 2: For any of link along y direction is faulty

```
if (j < l)
 if (i<(n-1)
```

Next positions are (i+1,j),(i+1,j+1),and (i-1,j+1)

else

Next positions are (i-1,j),(i-1,j+1),and (i+1,j+1)

else if(i<n-1)

Next positions are (i+1,j),(i+1,j-11),and (i-1,j-1)

else

Next positions are (i-1,j),(i-1,j-1),and (i+1,j-1)

Case 3: For any of wraparound link along x direction (w_x) is faulty

if(x=Mid-1)

Next position is (x+n-1,w_x)

else if(x<n-1)

Next position is (x+1,w_x)

else next position is (x-1,w_x)

Case 4: For any of wraparound link along y direction (w_y) is faulty

if(y=Mid-1)

Next position is (y+n-1,w_y)

else if(y<n-1)

Next position is (y+1,w_y)

else next position is (y-1, w_y)

C. Illustration of Fault-free Routing in FTT

Here, we illustrate the routing in a fault-free situation. Let us consider two sources source1(0,0), source2(3,0) and two destinations destination1(4,3) and destination2(2,4). The path is established according to the routing procedure and it is illustrated in Fig.2. The routing is based upon the selection of the shortest path between any source and destination. The black-shaded links as shown in the figure are the paths established from two sources to two destinations.

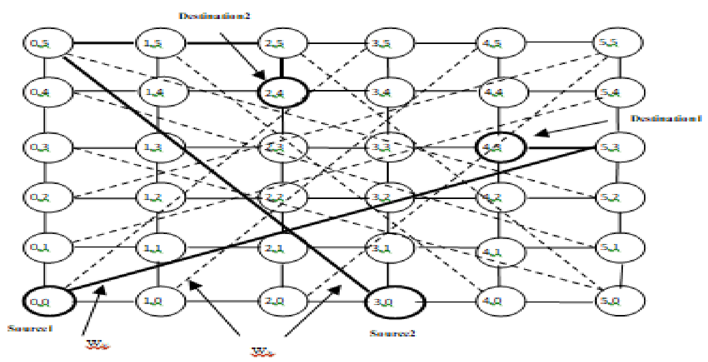

Figure 2: Illustration of Fault-free routing in FTT.

D.Illustration of Fault-tolerant Routing in FTT

Here, we illustrate the details of routing in the faulty situation. The fault can be tolerated by selecting an alternate path for forwarding of messages. The selection of the path is based upon the position of the current node. The fault-tolerant routing selects the next node position in presence of faulty paths. The different possible occurrences of faults are considered in the proposed fault- tolerant procedure. The fault may present along x axis, y axis, wx or wy. In this proposed routing method, all these four cases are considered and the technique of selection of alternate path is also proposed. This is illustrated in Fig. 3.

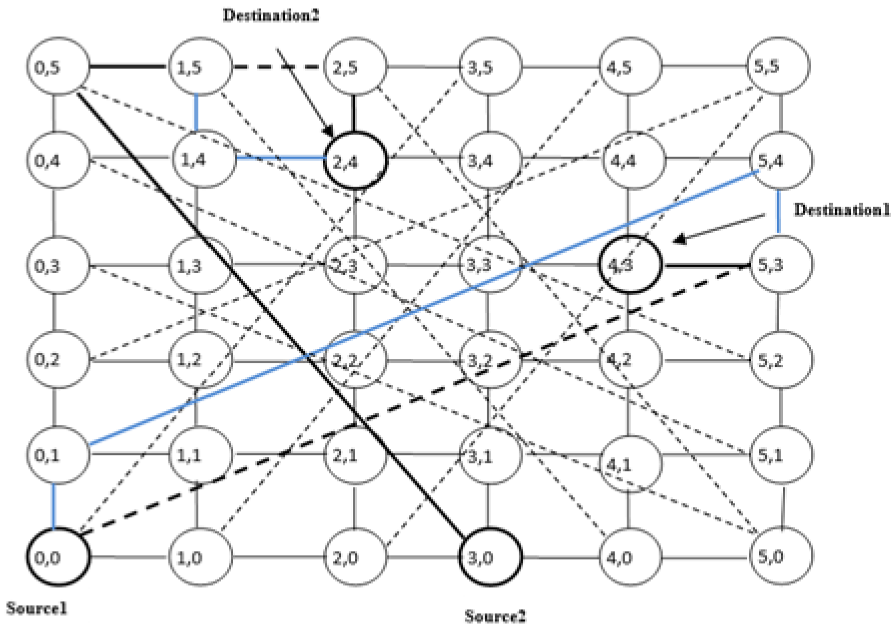

Figure 3: Illustration of Fault-Tolerant Routing in FTT.

6. Hamiltonian Cycle In Ftt

The proposed topology FTT satisfies the existence of the Hamiltonian Cycle which is also a desirable property of fault tolerance [31,33]. The network with the Hamiltonian cycle has fault tolerance capability. The Hamiltonian cycle is embedded in FTT which is illustrated in Fig.4.

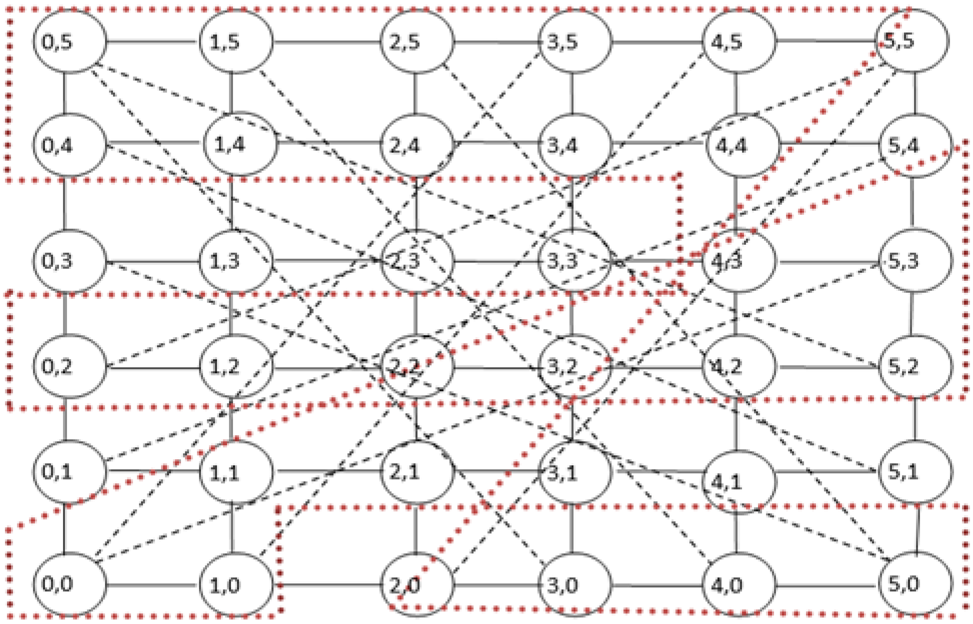

Figure 4: Illustration of the Hamiltonian cycle in FTT.

7. Performance Comparison

The performance analysis of FTT networks with existing networks is based upon the comparison of topological properties like network diameter, bisection width, average distance between two nodes, and packing density. The diameter of a topology affects the communication latency. The average distance between any two nodes is directlyproportional to the latency [26]. The efficient routing algorithm and ideal flow control mechanism have a direct impact on the throughput of a network [25]. As the network average distance affects latency in communication so, the desirable property of any topology is that the diameter and average distance should be less and the bisection width must be more. For a network, the packing density is defined as the total number of nodes per unit cost. It is related to the size of the VLSI chip design. The higher the packing density of a network the smaller the size of the VLSIchip.

"The excellent features of FTT over MCR, Mesh, TCR(27), and Octagon for Ubiquitous Computing (OUC)are shown in Table 1. In our discussion, the number of nodes is $N = 4k^2$. "

Table 1. Performancecomparison of FTT, TCR, Mesh, MCR, and OUC.

Topology	Mesh	MCR	TCR	OUC	FTT
Node degree	4	3	3	7	4

Average Distance	4k/3	4k/3	N	N/8	N
Network Diameter	2(2k-1)	6(k-1)	3k	N/8 + 1	2k-2
Bisection Width	2k	k	2k	N	6k
Network Cost	8(2k-1)	18(k-1)	9k	7(N/8 +1)	4(k-2)
Network Size	2k×2k	k×k	k×k	N×N	2k×2k
Packing Density	$k^2/2(2k-1)$	$2k^2/9(k-1)$	$2k^2/9(k-1)$	$4k^2/7(N/8+1)$	$4k^2/4(k-2)$

The average distance and diameter of FTT topology are the least of all other topologies discussed in Table 1. The bisection width of FTT is the highest among the rest of the topologies under consideration except OUC. As the diameter and node degree of FTT is less so, the cost is the lowest among all these topologies. The packing density of FTT is the highest among other topologies under consideration.The effect of various topological parameters is mentioned in Table 2.

Table 2. Numericalcomparisons.

Topology	Number of nodes	Degree	Diameter	Cost	Bisection Width	Packing density
Mesh	16	4	6	24	4	0.66667
	25	4	8	32	5	.78
	49	4	12	48	7	1.02
	64	4	14	56	8	1.388889
	81	4	16	64	9	1.26
	144	4	22	88	12	1.63
MCR	16	3	6	18	2	0.888
	36	3	12	36	3	1
	64	3	18	54	4	1.18
	100	3	24	78	5	1.38
	144	3	30	90	6	1.6
	196	3	36	108	7	1.81
	256	3	42	126	8	2.03
TCR	16	3	6	18	4	0.888
	36	3	9	27	6	1.333
	64	3	12	36	8	1.777
	100	3	15	45	10	2.222
	144	3	18	54	12	2.666
	196	3	21	63	14	3.111
	256	3	24	72	16	3.555

OUC	16	7	3	21	16	.76
	64	7	9	63	64	1.01
	144	7	19	133	144	1.08
	256	7	32	224	256	1.14
FTT	36	4	4	16	18	1.33
	64	4	6	24	24	2
	100	4	8	32	30	2.6
	144	4	10	40	36	3.11
	196	4	12	48	42	3.6
	256	4	14	56	48	4.11

FromTable 2, it is observed that the diameter and average distance of FTT are less than MCR and OUC and the bisection width of FTT is more than TCR and MCR but less than OUC. As the number of links in OUC is more and the degree of the router is 7 so, its cost and hardware complexity are more. As the bisection width of OUC is more so, the network will be less congested than other topologies under consideration. The cost of the OUC is the highest among all topologies under consideration. The network diameter is helpful in minimizing communication overhead [25]. If the network diameter of a topology is less so, the communication overhead will be less.

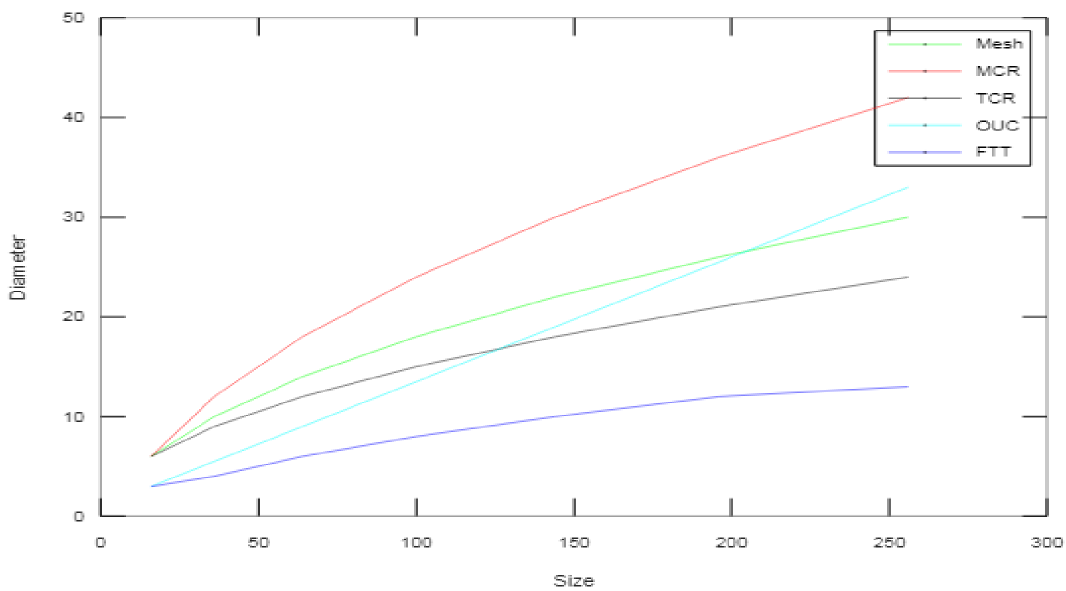

Figure 5: Comparison of Network Diameter Vs Number of nodes

The diameter analysis is shown in Fig.5. It reflects that if the node size increases the diameter of OUC, MCR, and Mesh increases more rapidly than TCR and FTT. For the small number of nodes, the diameter of OUC and FTT are less than other networks but as size increases the diameter of OUC will become larger than mesh, FTT, and TCR.

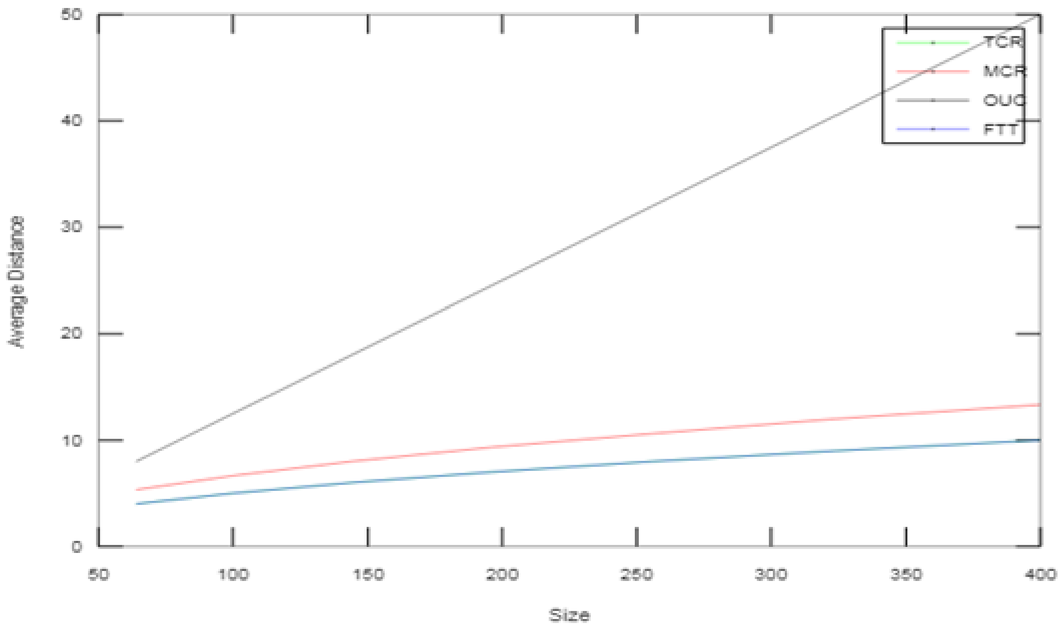

Figure 6: Comparison of Average distance Vs Number of nodes

"The average distance between any two nodes is shown in Fig.6. As the average distance of Mesh and MCR are the same, so, we take only MCR in our analysis. From the figure, it is observed that the average distance of both OUC and MCR is more than both FTT and TCR. The TCR and FTT have the same average distance. So, the time taken to reach any destination in both MCR and OUC is more than TCR and FTT."

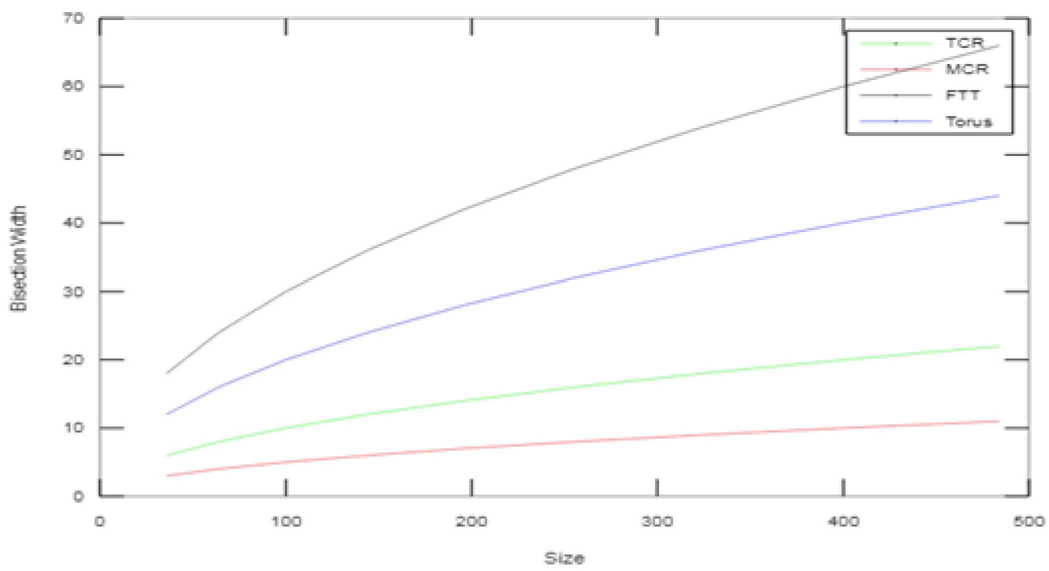

Figure 7: Comparison of Bisection Width Vs Size.

The effect of the bisection width of FTT and other networks with respect to thesize of the network is shown in Fig.7. It is observed from the analysis that the bisection width of FTT is the highest among all networks under consideration. It provides less congestion than existing networks.

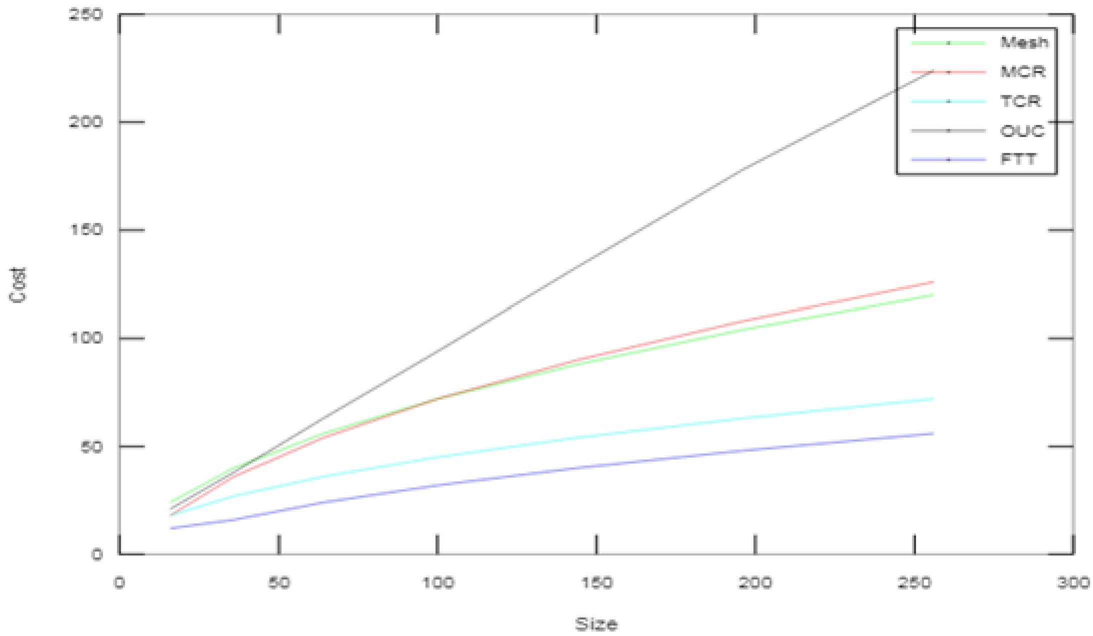

Figure 8: Comparison of Cost Vs Size.

"The Cost of FTT is always less than OUC, MCR, TCR, and Mesh. The cost analysis is reflected in Fig.8. For less number of nodes, all three topologies have approximately the same cost but as size increases the cost of FTT can be clearly distinguished from the other three topologies. "

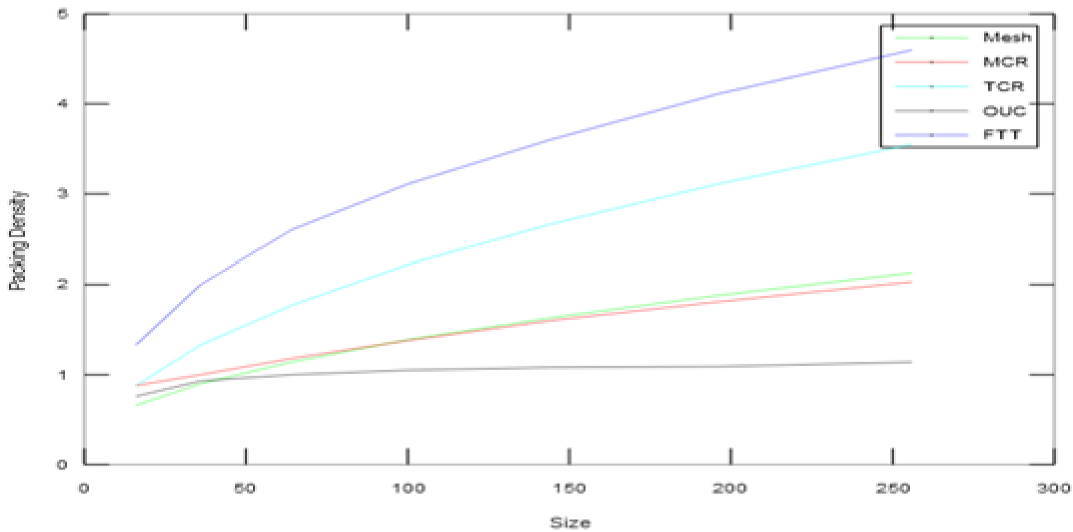

Figure 9: Comparison of Packing Density Vs Size.

"The packing density analysis is shown in Fig.9. It is observed that the packing density of FTT is the highest among all topologies under consideration which is also a desirable property for VLSI chip design. The higher packing density is suitable for designing the chip. The other topologies which use concentration versions like CMesh and CTorus have small diameter but due to hardware complexity, the cost is more in comparison to those of both TCR and MCR.

From Fig. 5, 6, and 8, it is clearly shown that if the size of the network increases then the average distance, diameter, and cost of FTT is lowest among MCR, OUC, TCR, and Mesh. The bisection width of OUC is N, where N is the number of nodes. As OUC has more degree than TCR so, it has more links and hence, its cost is more. "

8. Conclusion

In this paper, a Torus based new fault-tolerant interconnection network calledFully Twisted Torus (FTT) has been proposed. The proposed interconnection network is simple in structure, regular, and highly scalable. The said network hasbetter fault-tolerance capability. The topological properties like node degree, diameter, network cost, bisection width, and packing density of the proposed network were investigated and compared with other contemporary networks. The FTT is observed to be better than Mesh, Torus, MCR, and OUC in terms of node degree, network diameter, the average distance between any two nodes, packing density, bisection width, and network cost. The routing techniques in two distinct cases (i) Fault-free routing (ii) Fault-tolerant routing was presented are illustrated. The FTT is found to offer a high degree of fault tolerance. The presence of Hamiltonian cycles in both these networks was illustrated through suitable examples. We summarize below the results of the comparisons made in this paper.

(i) For any size of the network, the diameter of FTT is the lowest among all other networks.

(ii) The average distance between any pair of nodes in FTT isthe same and less than OUC and MCR.

(iii) The bisection width of the FTT is the highest among Torus, MCR, and TCR.

(iv) The cost of FTT is less than OUC, MCR, TCR, and Mesh.

(v) The packing density of the FTT network has the highest value among the rest of the networks under consideration.

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References

1 G. Henry, B. Cole, P. Fay, T.G. Mattson, "The Performance of the Intel TFLOPS Supercomputer," Intel Technology Journal, Q1'98, issue, 1998.

2 D. Lenoski, J. Laudon, K. Gharachorloo, WD Weber, A. Gupta, J. Hennessy, M. Horowitz, MS Lam, "The Stanford dash multiprocessor", Computer. vol. 25, no.3, pp.63-79, 1992.

3 S. S. Mukherjee, P. Bannon, S. Lang, A. Spink, and D. Webb, "The Alpha 21364 network architecture", IEEE Micro, vol. 22, no. 1, pp. 26–35, 2002.

4 N. R. Adiga et al. Blue Gene/L torus interconnection network. IBM Journal of Research and Development, vol.49 no.2/3, 2005.

5 A. Agarwal. Limits on interconnection network performance. IEEE Transactions on Parallel and Distributed Systems, 2(4):398–412, 1991.

6 S. R. Vangal, et al., "An 80-tile sub-100-w teraflops processor in 65-nm cmos," vol. 43, no. 1, 2008.

7 Oak Ridge National Laboratory. Introducing Titan: Advancing the Era of Accelerated Computing. Press release, November 2012. http:// www.olcf.ornl.gov / titan/

8 IBM. 20 Petaflop Sequoia Supercomputer. Press release, February 2009.

9 Y. Ajima, Tomohiro Inoue, SinyaHiramoto, and Toshiyuki Shimizu, "The Tofu Interconnect," IEEE Micro, vol. 32, no. 1, pp. 21–31, 2012.

10 W. J. Dally and B. Towles, "Route packets, not wires: on-chip interconnection networks", Proceedings of DAC, pp. 684-689, 2001.

11 ErnoSalminen, Ari Kulmala, and Timo D. H¨am¨al¨ainen. "Survey of Network-on-chip," white paper, OCP-IP, pp. 1-13, 2008.

12 Liu Youyao, Han Jungang, and Du Huimin., "DL(2m): A New Scalable Interconnection Network for System-on-Chip," Journal of Computers, vol. 4, no. 3, pp. 201-207, 2009.

13 B. Qiao, F. Shi, and W. Ji, "THIN: A new hierarchical interconnection network-on-chip for SOC," Proceedings of the 7th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP ' 07), pp. 446–457, 2007.

14 Wang Wei et al., "A Kind of Hierarchical Ring Interconnection Networks-on-Chip," Chinese Journal of Computer, vol. 33, no. 2, pp. 326-334, 2010.

15 Liu Youyao, Han Jungang, and Du Huimin., "DL(2m): A New Scalable Interconnection Network for System-on-Chip," Journal of Computers, vol. 4, no. 3, pp. 201-207, 2009

16 Zhu X J, Hu W W, Ma K, et al., "XMesh: mesh like topology for network on chip", Journal of Software, 2007, 18(9): 2194- 2204.

17 N. GopalakrishnaKini, M. Sathish Kumar, and H. S. Mruthyunjaya," A Torus Embedded Hypercube Scalable Interconnection Network for Parallel Architecture," IEEE International Advance Computing Conference (IACC) pp. 6-7 March 2009.

18 J .F. Fang, J.Y. Hsiao, and C. Y. Tang, "Embedding Meshes and TORUS Networks onto degree-four chordal rings," Proceedings of IEEE Conference on Computer and Digital Technology, vol. 145, no. 2, March 1998.

19 Zheng Wang, Huaxi Gu, Yawen Chen, Yintang Yang, Kun Wang, "3D network-on-chip design for embedded ubiquitous computing systems," Journal of Systems Architecture, 2016, pp. 1–8.. http: //dx.doi.org/10.1016/ j.sysarc.2016.10.002.

20 YG Wang, HM Du, XB Shen. Topological properties and routing algorithm for semi-diagonal torus networks. The Journal of China Universities of Posts and Telecommunications. 2011 October; 18(5):64-70.

21 Xinyu Wang, Dong Xiang, Zhigang Yu, "TM: a new and simple topology for interconnection Networks", journal of Supercomputing, vol.66, no.1, pp.514–538, 2013.

22 DeewakarThakyal and Pushpita Chatterjee, "DIA-TORUS:A novel topology for Network On Chip design," International Journal of Computer Networks & Communications (IJCNC) Vol.8, No.3, May2016, pp.137-148.

23 Liu Yu-hang, Zhu Ming-fa, Wang Jue, Xiao Li-min, Gong Tao, "Xtorus: An Extended Torus Topology for On-Chip Massive Data Communication", In proceedings of IEEE 26th International Symposium Workshops & PhD Forum on Parallel and Distributed Processing,pp.2061-2068,2012.

24 Manish Bhardwaj. C2 Torus New Interconnection Network Topology Based on 2D Torus. American Journal of Networks and Communications. Special Issue: Ad Hoc Networks. Vol. 4, No. 3-1, 2015, pp. 1-4. doi:10.11648/j.ajnc.s.2015040301.11.

25 J. Duato, S. Yalamanchili, , L Ni. "Interconnection Networks: an Engineering Approach," Publishing House of Electronics Industry, Beijing 2004.

26 Pablo Fuentes, Enrique Vallejo, Carmen Mart´ınez, Marina Garc´ıa, Ram´onBeivide, "comparison study of scalable and cost effective interconnection networks for HPC," In: 41st International Conference on Parallel Processing Workshops (ICPPW), 2012, pp.594-595.

27 Laxminath Tripathy and Chita Ranjan Tripathy, "A NEW INTERCONNECTION TOPOLOGY FOR NETWORK ON CHIP", International Journal of Computer Networks & Communications (IJCNC) Vol.10, No.4, 2018, pp.36-50.

28 Abhilasha Sharma and Sangeetha Rengachary Gopalan, "Performance analysis of torus optical interconnect with data centre traffic", ETRI Journal. WILEY,2020. DOI: 10.4218/etrij.2019-0318

29 SHENGHUI CHENG, WEN ZHONG, KATHERINE E. ISAACS, AND KLAUS MUELLER, "Visualizing the Topology and Data Traffic of Multi-Dimensional Torus Interconnect Networks," IEEE Access, VOLUME 6, 2018, pp. 57204-57204.

30 Jose´ M. Ca´mara, Miquel Moreto´, Enrique Vallejo, Ramo´nBeivide, Member, Jose´ Miguel-Alonso, Member, IEEE Computer Society, Carmen Martı´nez, and Javier Navaridas, "Twisted Torus topologies for Enhanced Interconnection Networks", IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS, Vol. 21, No. 12, 2010, pp.1765-1768.

31 YUXING YANG and LINGLING ZHANG, Prescribed Hamiltonian Connectedness of 2D Torus Journal of Interconnection Networks, Vol. 20, No. 01, 2020, https://doi.org /10.1142/ S021926592050 0012.

32 SATOSHI FUJITA, Three-Tier Delaunay Network as a Topology for Peer-to-Peer Overlay, Journal of Interconnection Networks,Vol. 19, No. 04, 2019. https://doi.org/10.1142/S0219265919500105.

33 Dongqin Cheng, Hamiltonian Cycles Passing Through Prescribed Edges in Locally Twisted Cubes, Journal of Interconnection Networks, VOL. 22, NO. 02, https://doi.org/10.1142/S0219265921500201.

34 R. Takahashi et al., Torus data centre network with smart flow control enabled by hybrid optoelectronic routers, IEEE/OSA J. Opt. Communication Network. 7 (2015), no. 12, B141–B152.

35 Gulzari UA, Sajid M, Anjum S, Agha S, Torres FS, A New Cross-By-Pass-Torus Architecture Based on CBP-Mesh and Torus Interconnection for On-Chip Communication. PLoS ONE 2016,11(12), 2016.